NAL/PUR/ALD/138/21-Z[0] 15-Nov-2021

PROCEEDINGS OF THE PRE-BID CONFERENCE HELD ON 15-Nov-2021 THROUGH WEBEX TOWARDS PROCUREMENT OF DESIGN, DEVELOPMENT, QUALIFICATION AND CERTIFICATION OF INPUT-OUTPUT MODULE (IOM) FOR IAFCC COMPUTER.

The Pre-bid Conference was held and the following T&PC members attended the meeting: -

Sl. No.	Name & Designation		Role
1	Dr. M. Manjuprasad	Chief Scientist, STTD	Chairman
2	Mr. Dilip Kumar Sahu,	Sr. Technical Officer-2, CAD	Member
3	Mr. Satish Rohidekar,R	Chief Scientist, CAD	Member
4	Mr. Vineet Kumar	Chief Scientist, CAD	PD-SARAS Member
5	Smt. S. Veena	Sr. Principal Scientist, ALD	Member - Convener (TSC)

The list of Prospective bidders who attended the Pre-bid Conference is as per **Annexure-I.**

At the outset, the Chairman welcomed all the Members and the representatives of the Bidders and briefed in general the scope of the Project. The Indenting Officer to read out the clarification sought by the bidders and the replied thereto as detailed in **Annexure-II (Part A: Technical Clarification and Part B: Commercial Clarification, if any).**

The representatives present were satisfied with the replies given and it was informed that the corrections / additions / clarifications given, as discussed during the Pre-Bid Conference would be hosted on the website of CSIR-NAL and all prospective bidders are required to take cognizance of the proceedings of the Pre-Bid Conference before formulating and submitting their bids as stipulated in bidding Documents.

The meeting ended with a vote of thanks to the Chair.

Encl: as above.

Dilip Kumar Sahu
Member

R. Satish Rohidekar
Member

Vineet Kumar
Member 22/Nov/2021

S. Veena
Member – Convener (TSC)

Dr. M. Manjuprasad
Chairman-T&PC

CSIR-NATIONAL AEROSPACE LABORATORIES
BENGALURU - 560 017

TENDER NO.: NAL/PUR/ALD/138/21-Z[O] **ANNEXURE - I**
DATE & TIME : 15-Nov-2021 @ 11.00 am
VENUE: THROUGH WEBEX

Pre-Bid Conference for Design, Development, Qualification and Certification of Input-Output Module (IOM) for IAFCC computer

ATTENDANCE SHEET - T&PC MEMBERS

Sr. No.	Name		Signature
1	Dr. M. Manjuprasad, Chief Scientist, STTD	Chairman	
2	Mr. Dilip Kumar Sahu, Sr. Technical Officer-2, CAD	Member	
3	Mr. R. Satish Rohidekar, Chief Scientist, CAD	Member	
4	Mr. Vineet Kumar, Chief Scientist, CAD	Member	
5	Smt. S. Veena, Sr. Principal Scientist, ALD	Member- Convenor -TSC	
6	Dr. Ananda C M	Head, ALD	
7	Mr. Venkatesh K S	Co PL, IAFCC	
8	Mr. Pradeep Kumar	Co PL, IAFCC	

NATIONAL AEROSPACE LABORATORIES
BENGALURU - 560 017

TENDER NO.: NAL/PUR/ALD/138/21-Z[O] ANNEXURE - I
DATE & TIME : 15-Nov-2021 @ 11.00 AM
VENUE:

Pre-Bid Conference for Design, Development, Qualification and Certification of Input-Output Module (IOM) for IAFCC Computer

ATTENDANCE SHEET - PROSPECTIVE BIDDERS

Sr. No.	Name of the Firm	Name & Designation of Representative	E-tender Registration (Yes/No)	Email ID
1	CoreEL Technologies	1. Aravind Pamali, Director- Strategic Projects 2. Sairam Patro, Director – Systems Engineering 3. Damodar Baliga, Business Development Manager		damodar.b@coreel.com
2	Mistral Solutions	1. Taxal Shenai, Account Manager- Sales 2. Srikanth 3. Mateer Bhat		taxals@mistralsolutions.com
3	Avench Systems Private Limited	1. Arsalan Ather,Account Manager 2. Diljet, CTO 3. Bijesh, Technical Manager 4. Rajeend, V P Sales 5. Shillka, Pre-Sales Engineer		1) arsalan@avench.com 2) diljith.m@avench.com 3) bijesh.t@avench.com

CSIR-NATIONAL AEROSPACE LABORATORIES
BENGALURU

TECHNICAL QUERIES & CLARIFICATION

Tender No. : **NAL/PUR/ALD/138/21-Z[0]**

Item Description :

Sr. No.	Query / Clarification Sought	Clarification/Amendment
1.	Recommended FPGA part number to be provided	Bidder may consider Xilinx Artix 7 series Suggested Part Nos XC7A100T for FPGA 1 XC7A50T for FPGA 2 Note: Bidder has the option to choose an alternative Part no from the same family, provided the alternate part no. fulfils requirements.
2.	Is FPGA development (PL Design: please give full form of PL) activity a part of vendors responsibility?	No, Vendor shall not be responsible for any PL design of FPGA, however Vendor shall demonstrate that the data is available inside FPGA for all inputs by using test codes for each type of interface to prove that data from each data type is available to the FPGA.
3.	Is DO 254 certification and documentation scope of the vendor	No Complete DO 254 certification life cycle process is in NAL's scope, No cost to be included for this in tender costing.
4.	Are only Board Level Screening (BLS) and ESS to be done by the Vendor.	Yes. BLS to be done for functional boards before delivery. ESS to be carried out on production version of IO module before delivery Note : 1. ESS will be carried out with test codes developed by NAL and vendor need not consider any test code development charges for ESS. 2. QT will be carried out along with the NAL's Computer with the IO Module integrated. Vendor shall support till the complete qualification tests are successful. NAL shall carryout the complete Qualification Tests as per DO 160 G and hence vendor shall not consider testing efforts(budget).
5.	Delivery time line for phase I is still a concern, and NAL will confirm on the phase 1 deliverables. (if it is 6+1 Proto for CDR).	Based on the feedback from majority of Vendors, the Phase I timelines is revised from 6 months to 8 months. Phase I will include the CDR stage.

		Hence accordingly the Phase II timeline to deliver 18 Qualified IOM is revised from 12 months to 10 months Also it is suggested that one prototype IOM using commercial components (commercial/non-qualified version) shall be delivered before CDR to prove (what's the scope of 'prove' ?) the design. Vendor shall consider this also as part of schedule and efforts.
6.	Section 4.4.3: Installation, Commissioning and ATP : Will ATP happen at NAL	Yes The detailed ATP shall be conducted at CSIR NAL premises using NAL's Test Facility for carrying out the ATP. However, the minimum tests required at Vendors premises to prove the functioning of the IOM shall be tested by vendors at vendor's premises before the IOM is delivered to NAL for ATP.
7.	In Section 4.2.2, point No. C in table, description regarding differential signal is mentioned. Kindly let us know are the inputs to the I/O card single ended or differential?	Based on the pin count demand at the backplane (connecting the IO termination panel and Backplane), the decision of converting the differential to Single ended shall be taken at PDR level, This information shall be provided to the vendor at the design stage. However, in any case the maximum pinouts of IOM shall be as per VITA standards.
8.	Section4.2.2, subsection g, point No. ii : Is IPC 610 Class III with group B required only for production series IOM qty 18 Nos or to both production and functional IOM – total 24 Nos ?	It is required for 24 cards and it is not required for functional prototype
9.	Section4.2.3-point No. 6 : Kindly provide details regarding the tests involved in module level qualification tests. Are these tests to be done during operation of the IOM or non-operational?	**BLS tests** 1. Storage test 2. Thermal shock 3. Temperature variation test **ESS test sequence** 1. Vibration test 2. Temperature variation test Test procedure and test sequence to be arrived at in discussion with certification agency after review.
10.	In order to successfully achieve the objective of this RFQ, the bidder needs to work closely with the partner of CSIR-NAL who is developing IAFCC. CSIR-NAL will help in coordination wherever required. This mode of 'closed loop' functioning will help greatly in qualification of the I/O modules with IAFCC features.	

Veena. S.

Signature of IO & PL 23/11/21

CSIR-NATIONAL AEROSPACE LABORATORIES
BENGALURU

COMMERCIAL QUERIES & CLARIFICATION

Tender No. : NAL/PUR/ALD/138/21-Z[O]
Item Description : Design, Development, Qualification and Certification of Input-Output Module (IOM) for IAFCC computer

Query / Clarification Sought	Clarification/Amendment
— NIL —	

24-11-21

Sr. Controller of Stores & Purchase
For and on behalf of CSIR